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NOTICE OF ALLOWANCE AND FEE(S) DUE

50170 7590 09/16/2009

IBM CORP. (WIP)
c/o WALDER INTELLECTUAL PROPERTY LAW, P.C.
17330 PRESTON ROAD
SUITE 100B
DALLAS, TX 75252

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/16/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,553	03/25/2004	Charles Ray Johns	AUS920030696US1	7923

TITLE OF INVENTION: METHOD TO PROVIDE CACHE MANAGEMENT COMMANDS FOR A DMA CONTROLLER

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	12/16/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

50170 7590 09/16/2009

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c/o WALDER INTELLECTUAL PROPERTY LAW, P.C.
17330 PRESTON ROAD
SUITE 100B
DALLAS, TX 75252

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

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10/809,553	03/25/2004	Charles Ray Johns	AUS920030696US1	7923

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nonprovisional	NO	$1510	$300	$0	$1810	12/16/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEE, CHUN KUAN	2181	710-022000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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LEE, CHUN KUAN	
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DATE MAILED: 09/16/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 1177 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 1177 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/809,553	JOHNS ET AL.	
	Examiner	Art Unit	
	Chun-Kuan Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *06/15/2009*.

2. ☒ The allowed claim(s) is/are *1, 9, 15 and 22-36 (renumbered as claims 1-18)* .

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 02/09/2009
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Niketa I. Patel/
Primary Examiner, Art Unit 2181

DETAILED ACTION

I. EXAMINER'S AMENDMENTS

OPTIONS AVAILABLE TO THE APPLICANT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by **37 CFR § 1.312**. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

AUTHORIZATION FOR THE CORRECTIONS BY THE EXAMINER

2. Authorization for this examiner's amendment was given in a telephone interview with Stephen Tkacs, having Reg. No. 46,430, on 09/11/2009. Accordingly, since a complete record of the interview has been incorporated in the instant examiner's amendment, no separate interview summary form is included in the instant office letter **MPEP § 713.04**.

CORRECTIONS MADE IN THE APPLICATION

The application has been amended as following:

IN THE CLAIMS:

The below described amendments to the claims are necessary to further clarify the claimed invention.

NOTE: The claims amended by this examiner's amendment have been referred to by their original claim number and, if renumbered at time of allowance, also by the new number located in parentheses as required by **MPEP § 1302.04(g)**.

3. In claim 1, "... A system to provide software program control of cache management, comprising:

a processor configured to generate DMA commands for the management of a cache on the execution of a software program on the processor; and

a DMA controller coupled to the processor, configured to execute the DMA commands for the management of a cache ..."

should be replaced with

-... A system to provide software program control of cache management, comprising:

a control processor;

one or more asymmetric processors;

a shared system memory;

one or more local memories, wherein each of the one or more local memories is associated with a respective one of the one or more asymmetric processors;

a direct memory access (DMA) controller coupled to the control processor and the one or more asymmetric processors, configured to execute DMA commands a for moving data between the shared system memory and the one or more local memories; and

a DMA cache coupled to the DMA controller configured to cache data being moved between the shared system memory and the one or more local memories;

wherein the control processor is configured to generate DMA cache management commands for the management of the DMA cache;

wherein the DMA cache management commands comprise at least one of a data cache range touch command that indicates to the DMA controller that the control processor will probably issue a get command for a specified address range, a data cache range touch for store command that indicates to the DMA controller that the control processor will probably issue a put command for a specified address range, a data cache range set to zero command that sets a range of storage specified by an effective address and transfer size to zero, a data cache range store command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory if the data block is considered modified, and a data cache range flush command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory and invalidated in caches of all processors if memory coherency is required and the data block is modified ...-.

4. Claims 2-8 are canceled.

5. In claim 9 (renumbered as claim 7), "... A method for cache management in a system comprising a DMA controller and a processor, the method comprising the steps of:

running software on the processor to generate DMA commands for management of a cache;

issuing the DMA commands to the DMA controller; and

executing the DMA commands ..."

should be replaced with

-... A method for cache management in a system comprising a DMA controller and a processor, the method comprising the steps of:

running software on a control processor to generate direct memory access (DMA) commands for moving data between a shared system memory and one or more local memories, wherein each of the one or more local memories is associated with a respective one of one or more asymmetric processors;

issuing the DMA commands to the DMA controller; and

executing the DMA commands, wherein the DMA controller is coupled to a DMA cache configured to cache data being moved between the shared system memory and the one or more local memories,

wherein the control processor is configured to generate DMA cache management commands for the management of the DMA cache;

wherein the DMA cache management commands comprise at least one of a data cache range touch command that indicates to the DMA controller that the control processor will probably issue a get command for a specified address range, a data cache range touch for store command that indicates to the DMA controller that the control processor will probably issue a put command for a specified address range, a

data cache range set to zero command that sets a range of storage specified by an effective address and transfer size to zero, a data cache range store command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory if the data block is considered modified, and a data cache range flush command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory and invalidated in caches of all processors if memory coherency is required and the data block is modified ... -.

6. Claims 10-14 are canceled.

7. In claim 15 (renumbered as claim 13), "... A computer program product for cache management in a system comprising a DMA controller and a processor, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for running software on the processor to generate DMA commands for management of a cache;

computer code for issuing the DMA commands to the DMA controller; and computer code for executing the DMA commands ..."

should be replaced with

-... A computer program product for cache management in a system comprising a DMA controller and a processor. the computer program product having a computer

storage medium with a computer program embodied thereon, the computer program comprising:

computer code for running software on a control processor to generate DMA commands for moving data between a shared system memory and one or more local memories, wherein each of the one or more local memories is associated with a respective one of one or more asymmetric processors;

computer code for issuing the DMA commands to the DMA controller; and

computer code for executing the DMA commands, wherein the DMA controller is coupled to a DMA cache configured to cache data being moved between the shared system memory and the one or more local memories,

wherein the control processor is configured to generate DMA cache management commands for the management of the DMA cache;

wherein the DMA cache management commands comprise at least one of a data cache range touch command that indicates to the DMA controller that the control processor will probably issue a get command for a specified address range, a data cache range touch for store command that indicates to the DMA controller that the control processor will probably issue a put command for a specified address range, a data cache range set to zero command that sets a range of storage specified by an effective address and transfer size to zero, a data cache range store command that indicates a data block specified by an effective address and transfer size to be written to the shared system memory if the data block is considered modified, and a data cache range flush command that indicates a data block specified by an effective address and

transfer size to be written to the shared system memory and invalidated in caches of all processors if memory coherency is required and the data block is modified.

8. Claims 16-21 are canceled.

9. New claim 22 (renumbered as claim 2) is added as following "... The system of claim 1, wherein responsive to receiving the data cache range touch command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch command into the DMA cache ...".

10. New claim 23 (renumbered as claim 3) is added as following "... The system of claim 1, wherein responsive to receiving the data cache range touch for store command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch for store command into the DMA cache ...".

11. New claim 24 (renumbered as claim 4) is added as following "... The system of claim 1, wherein responsive to receiving the data cache range set to zero command, the DMA controller gets ownership of cache lines associated with an area of the shared system memory and zeroes data in the DMA cache such that the area of shared system memory is effectively zeroed ...".

12. New claim 25 (renumbered as claim 5) is added as following "... The system of claim 1, wherein responsive to receiving the data cache range store command, the DMA controller writes the data block to the shared system memory if the data block is modified ...".

13. New claim 26 (renumbered as claim 6) is added as following "... The system of claim 1, wherein responsive to receiving the data cache range flush command, the DMA controller writes the data block to the shared memory and invalidates the data block in caches of all processors if memory coherency is required and the data block is modified ...".

14. New claim 27 (renumbered as claim 8) is added as following "... The method of claim 9, wherein responsive to receiving the data cache range touch command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch command into the DMA cache ...".

15. New claim 28 (renumbered as claim 9) is added as following "... The method of claim 9, wherein responsive to receiving the data cache range touch for store command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch for store command into the DMA cache ...".

16. New claim 29 (renumbered as claim 10) is added as following "... The method of claim 9, wherein responsive to receiving the data cache range set to zero command, the DMA controller gets ownership of cache lines associated with an area of the shared system memory and zeroes data in the DMA cache such that the area of shared system memory is effectively zeroed ...".

17. New claim 30 (renumbered as claim 11) is added as following "... The method of claim 9, wherein responsive to receiving the data cache range store command, the DMA controller writes the data block to the shared system memory if the data block is modified ...".

18. New claim 31 (renumbered as claim 12) is added as following "... The method of claim 9, wherein responsive to receiving the data cache range flush command, the DMA controller writes the data block to the shared memory and invalidates the data block in caches of all processors if memory coherency is required and the data block is modified ...".

19. New claim 32 (renumbered as claim 14) is added as following "... The computer program product of claim 15, wherein responsive to receiving the data cache range touch command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch command into the DMA cache ...".

20. New claim 33 (renumbered as claim 15) is added as following "... The computer program product of claim 15, wherein responsive to receiving the data cache range touch for store command, the DMA controller attempts to bring the range of data identified by an effective address and transfer size of the data cache range touch for store command into the DMA cache ...".

21. New claim 34 (renumbered as claim 16) is added as following "... The computer program product of claim 15, wherein responsive to receiving the data cache range set to zero command, the DMA controller gets ownership of cache lines associated with an area of the shared system memory and zeroes data in the DMA cache such that the am of shared system memory is effectively zeroed ...".

22. New claim 35 (renumbered as claim 17) is added as following "... The computer program product of claim 15, wherein responsive to receiving the data cache range store command, the DMA controller writes the data block to the shared system memory if the data block is modified ...".

23. New claim 36 (renumbered as claim 18) is added as following "... The computer program product of claim 15, wherein responsive to receiving the data cache range flush command, the DMA controller writes the data block to the shared memory and

invalidates the data block in caches of all processors if memory coherency is required and the data block is modified ...".

II. DISTINGUISHING FEATURES RECITED IN THE CLAIMS

ALLOWABLE SUBJECT MATTER

24. Claims 1, 9, 15 and 22-36 (renumbered as claims 1-18) are allowed.

The following is an **Examiner's Statement of Reasons for Allowance**, **See MPEP 1302.14**:

25. The primary reason for allowance of independent claims 1, 9 and 15 (renumbered as claims 1, 7 and 13 respectively) in the instant application is in response to the decision from the Board of Patent Appeals and Interferences dated 06/15/2009 and applicant's amendments of the independent claims 1, 9 and 15 (renumbered as claims 1, 7 and 13 respectively). Because new claims 22-36 (renumbered as claims 2-3, 8-12 and 14-18) depend directly on independent claims 1, 9 and 15 (renumbered as claims 1, 7 and 13 respectively), these claims are considered allowable for at least the same reasons noted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.K.L./

September 11, 2009

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Niketa I. Patel/

Primary Examiner, Art Unit 2181